i4000

Quad M-module carrier for VMEbus

Hardware Manual

Revision 3.0

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Contents

1. Using the manual

This manual serves as instruction for the operation of the VMEbus board i4000, the connection of peripheral devices and the integration in a VMEbus system. Furthermore it gives the user additional information for special applications and configurations of the assembly.

Detailed information concerning the individual assemblies (data sheets etc.) are not part of this manual. In the annex you will find a bibliography.

This manual describes the hardware of the assembly.

Notes concerning the nomenclature:

Hex numbers are marked with a leading "$"-sign: for example: $800000 or $BFFFFF.

Active-low signals are represented by a trailing asterisks (i.e. IACK*).

1.1. Validity of this manual

The contents of this manual is valid for i4000 revision 2.x

1.2. Ordering considerations

The i4000 comes in two types: with, or without the P2 connector mounted.

Order Code	Description
i4000/P2	i4000 with P2 connector mounted
i4000/NP2	i4000 without P2 connector mounted

One should NOT apply the i4000/P2 when:

- a P2 backplane is in the VMEbus rack, or
- galvanic isolation is required.

NOTE: P2 connector on the i4000 is NOT VMEbus compatible !!!

2. Introduction

The i4000 is a modular passive peripheral-controller for the VME-bus. Up to four M-modules can be connected to the board to form a peripheral-controller..

2.1. Technical overview

The i4000 has the following features:

- 4 M-module slots
- One VMEbus slot needed
- short or standard VMEbus addressing (A16/A24)
- byte or word data transfer (D08/D16)
- D08(O) VMEbus interrupter
- peripheral I/O connections either up front or via the VME-P2 connector.
- Additional mounting holes to secure the modules

2.2. Block diagram

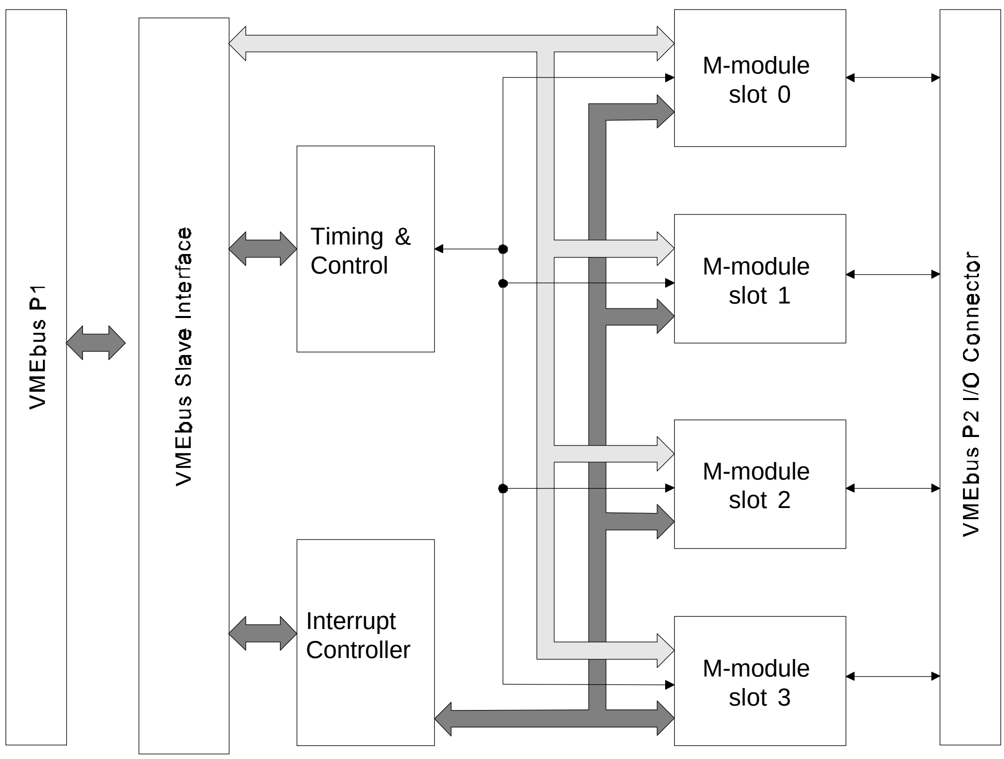

Figure 1 i4000 Block Diagram

3. VMEbus interface

3.1. Address interface

The i4000 can be selected to accept either short addressing, using 16 bit addresses (A16) or standard addressing, using 24 bit addresses (A24).

When using short addressing up to 32 i4000 boards can be put in a single VMEbus system since the lower 11 address lines (A0-A10) are used internally on the i4000. If standard addressing is used, a larger address space is available to select the board.

The memory space occupied by the i4000 is $800 bytes long. This memory space is equally spread across the four modules. so each module occupies $200 bytes. From these $200 bytes address space half is used by the interrupt controller. The address space for each module is therefore $100 bytes long (8 bit addressing).

The address space of the i4000 is selectable using dip switches (SW1 and SW2) which are accessible even when the four module slots are occupied. When a switch is "on" the corresponding address line is a logical "zero" and when a switch is "off" the corresponding address line is "one".

Address modifier AM4 can be used to select either standard or short memory addressing. If AM4 is "one" (the switch is in the off position) standard addressing is selected. If AM4 is "zero" (switch on) short addressing is selected. When using short addressing the address lines A16-A23 are don't cares.

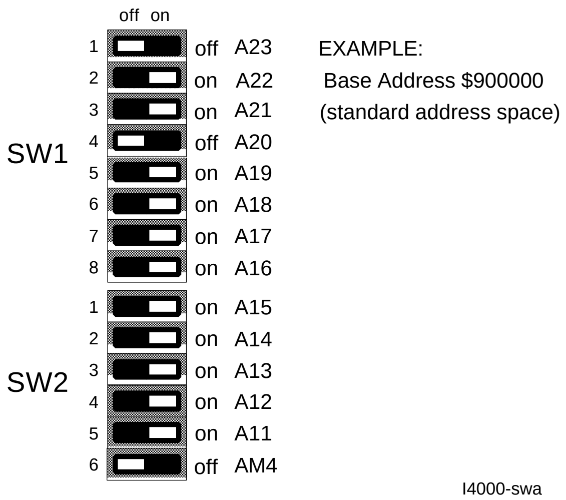

Figure 2 Address Selection

3.2. The interrupter

The i4000 has a special interrupter which is largely compatible with the M68C153. The interrupter is a so called D08(O) type interrupter which means that the interrupter during an interrupt acknowledge cycle will put a status byte on the data line D0-D7. The interrupter has one interrupt level (IRQ1-IRQ7) selectable by dip switches (SW3) for all the modules. Each module can generate its own vector.

There are two classes of interrupters which are both supported by the i4000: release on acknowledge (ROAK) or release on register access (RORA). The ROAK interrupter negates its interrupt request line in response to an interrupt acknowledge cycle. This mechanism will work with all handlers. The RORA interrupter releases its request when the handler accesses an on-board register during the interrupt service routine. The handler performs the acknowledge cycle but the interrupter does not immediately negate its request. Sometime during the service routine the handler will have to write to a register on the interrupter which causes it to negate the request.

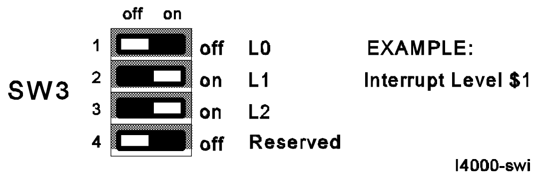

Figure 3 Interrupt request Level

3.3. Dipswitch locations

The location of the dip switches to select the base address (SW1 and SW2) and the dip switch to select the interrupt request level (SW3) can be found at the following locations:

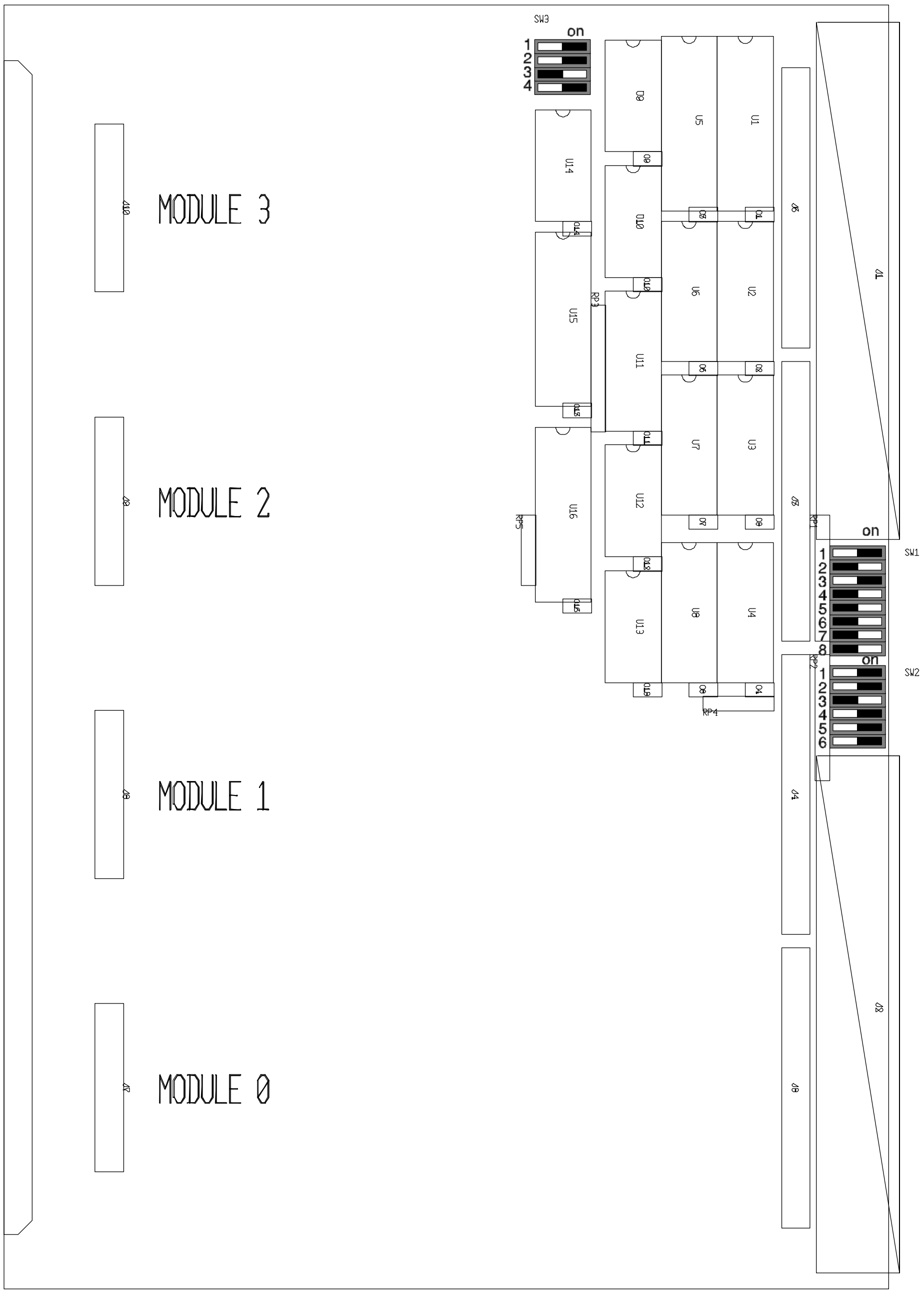

Figure 4 Dip switch locations

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3.4. VMEbus P1 connector assignments

The following table provides signal names for the VMEbus P1 connector as used by the i4000. (The connector consists of three rows of pins labelled rows a, b and c.)

Pin	Row A	Row B	Row C
01	D00		D08
02	D01		D09
03	D02		D10
04	D03	BG0IN*	D11
05	D04	BG0OUT*	D12
06	D05	BG1IN*	D13
07	D06	BG1OUT*	D14
08	D07	BG2IN*	D15
09	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	
11	GND	BG3OUT*	
12	DS1*		RESET*
13	DS0*		LWORD*
14	WRITE*		AM5
15	GND		A23
16	DTACK*		A22
17	GND		A21
18	AS*		A20
19	GND		A19
20	IACK*	GND	A18
21	IACKIN*		A17
22	IACKOUT*		A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V		+12V
32	+5V	+5V	+5V

4. Module installation

4.1. Mounting the module

A maximum of four modules can be fitted on the i4000 base board. To plug in a module slide the module from above under an angle on top of the i4000 and first position the 25-pole sub-D connector through the openings in the front cover. Then position the 24-pole female header on top of the corresponding header on the base board. Push the module until the 40-pole header connector is positioned and press the module with care in its place.

The module can be secured in its position using two or four screws (M3 * 5mm). The older modules only have mounting provisions for the two screws on the 25-pole sub-D connector but the newer modules have two additional screws to secure the module.

4.2. P2 connector assignments

Peripherals can be connected to M-modules in two ways. On the front side of the module a 25-pole sub-D connector (or mechanically equivalent) can be used to connect cables on the front panel of the VMEbus base board. Alternatively, a 24-pole header connector interfaces the I/O signals to the base board where they are connected to the VMEbus P2 connector.

In 32 bit VMEbus systems the backplane for the P2 connector must either be removed for the i4000 slot or an i4000 without the P2 connector must be ordered. In that case the peripherals can be connected to the M-module up front.

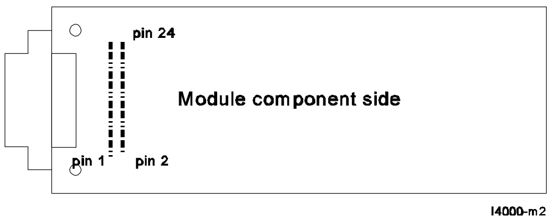

Figure 5 Orientation of 24-pole header connector

Every M-module has 24 pins of the P2 connector assigned. Four modules on a base board can then use this I/O path.

This division into four pads of the P2 connector enables so called "module connector" to be plugged into the back of a 96-way shroud, mounted on the "P2-backplane". On the 96-way connector 3 pins are not used for every module. Several manufacturers produce these "module connectors, which can be coded and sometimes have latches.

Corresponding pins on the 96-way P2 to 24-way header connector on module.

pin	Row c	Row b	Row a
01	3	2	1
02	6	5	4
03	9	8	7
04	12	11	10
05	15	14	13
06	18	17	16
07	21	20	19
08	(24)	(23)	(22)
09	3	2	1
10	6	5	4
11	9	8	7
12	12	11	10
13	15	14	13
14	18	17	16
15	21	20	19
16	(24)	(23)	(22)
17	3	2	1
18	6	5	4
19	9	8	7
20	12	11	10
21	15	14	13
22	18	17	16
23	21	20	19
24	(24)	(23)	(22)
25	3	2	1
26	6	5	4
27	9	8	7
28	12	11	10
29	15	14	13
30	18	17	16
31	21	20	19
32	(24)	(23)	(22)

4.3. i4000 - module interface connector assignments

The interface between the i4000 baseboard and a M-Module is realised with a 20-pole male header connector.

Pin	Row A	Row B
01	CS*	GND
02	A01	+5V
03	A02	+12V
04	A03	-12V
05	A04	GND
06	A05	DREQ*
07	A06	DACK*
08	A07	GND
09	D08	D00
10	D09	D01
11	D10	D02
12	D11	D03
13	D12	D04
14	D13	D)5
15	D14	D06
16	D15	D07
17	DS1*	DS0*
18	DTACK*	WRITE*
19	IACK*	IRQ*
20	RESET*	SYSCLK

Location of the 24-pole header connector on the M-module:

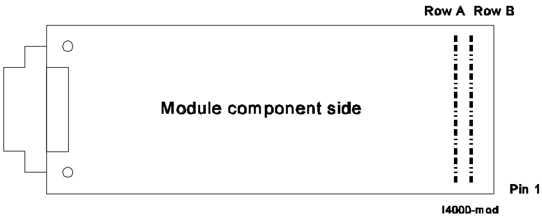

Figure 6 Orientation of connector on module

5. Software issues

5.1. Address mapping

As mentioned before the address space occupied by the i4000 board is $800 bytes (A0-A10). These $800 bytes are divided into 4 identical spaces. Every $200 bytes block is assigned to a module slot. The first $100 byte address space is assigned to the module itself and the second $100 byte is used for the access part of the interrupt controller.

Using this method of address decoding provides an identical address map for each module on the i4000 board. This makes writing the software easier since just the base address of the module, not the base address of the i4000 has to be known. Every module has its own Interrupt-Vector and Interrupt-Control register. The $100 bytes from each module used to access the interrupt controller are not completely decoded. Both registers of the Interrupt controller are mirrored several times within the $100 bytes address space. If the module itself the $100 bytes completely decodes, depends on the used module.

Address Map of the i4000:

$000..$0ff $101 $103	Module Control register (CR0) Vector register (VR0)	Module 0
$200..$2ff $301 $303	Module Control register (CR1) Vector register (VR1)	Module 1
$400..$4ff $501 $503	Module Control register (CR2) Vector register (VR2)	Module 2
$600..$6ff $701 $703	Module Control register (CR3) Vector register (VR3)	Module 3

The base address of a module can be calculated using the following formula:

ModuleBaseAddress = i4000BaseAddress + ModuleNumber * $200

EXAMPLE:

The installed base address of the i4000 is $800000. A module is fitted into slot 2. The module base address is then $800000 + 2 * $200 = $800200. When using a 32 bit master which accesses the standard address space at address $ffxxxxxx, then the module will be accessed at address $ff800200. The corresponding interrupt control register address is then $ff800301.

5.2. The interrupt controller

5.2.1. Functional description

The Interrupt controller used with the i4000 is largely compatible the MC68153 Interrupt controller from Motorola.

The interrupt controller provides a means for the modules to ask for an interrupt of the processor activity and receive service from the processor. The Interrupt controller on the i4000 acts as an interface device requesting and responding to interrupt acknowledge cycles for up to 4 independent modules.

5.2.2. Register description

The Interrupt controller of the i4000 contains 8 programmable registers. There are four control registers (CR0-CR3) that govern operation of the Interrupt controller and four vector registers (VR0-VR3) that contain the vector data used during an interrupt acknowledge cycle. Every module is assigned one register pair.

5.2.3. Control register

Control Register

7	6	5	4	3	2	1	0
RES	RES	X/IN	IRE	IRAC	L2	L1	L0
reset:							
u	u	u	u	u	u	u	u

Write only

L2-L0 (Interrupt level, dummy bits)

The least significant 3-bit field of the register determines the level at which an interrupt will be generated.
These three bits are NOT used in the i4000 interrupt controller since the interrupt level for all the four modules is selected via dip switches. However to maintain software compatibility with the A201 it is advisable to program these 3 bits with the same interrupt level as the dip switches.

IRAC (Interrupt Auto-Clear)

If the IRAC is set (Bit 3), IRE (Bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the module interrupt request. To re-enable the module interrupt request associated with this register, IRE must be set again by writing to the control register.

IRE (Interrupt enable)

This field (Bit 4) must be set (high level) to enable the module interrupt request associated with the control register. Thus, if the module asserts IRQ and IRE is cleared, no interrupt request to the VMEbus will be generated.

X/IN* (External/Internal)

Bit 5 of the control register determines the response of the i4000 interrupt controller during an interrupt acknowledge cycle. If the X/IN* bit is clear (low level) the Interrupt Controller will respond with vector data and a DTACK* signal, i.e., an internal response. If X/IN* is set, the vector is not supplied and no DTACK* is given by the Interrupt Controller, i.e., an external module should respond.

RESERVED

These two bits are not used in the current implementation of the Interrupt Controller and reserved for future use.

5.2.4. Vector registers

Each module interrupt input has its own associated vector register. Each register is 8 bits wide and supplies a data byte during its interrupt acknowledge cycle if the associated External/Internal (X/IN*) control register bit is clear (zero). This data can be status, identification, or address information depending on system usage. The information is programmed by the system user.

5.2.5. Interrupt controller reset

When a VMEbus reset is applied, the control registers of the i4000 interrupt controller are set to all zeros (low). The vector registers however are uninitialized and should be programmed before use.

6. Annex

6.1. Bibliography

Specification for M-module interface and physical dimensions:
M-module specification manual, revision 2.2, M-Module Manufactures Group.

Interrupt controller:
MC68153 datasheet, Motorola Semiconductors, Inc

6.2. Difference compared to former versions

Revision 1.0
- First release.

Revision 1.1
- Bug fixed concerning Interrupt level switch. Most significant and least significant bit are swapped.

Revision 2.0
- Jumpers removed
- Power and ground plane
- IACK's synchronized

6.3. Technical data

Module number:
Up to four modules can be plugged onto the baseboard. Virtually unlimited number of baseboards in one VME system.

Interrupt Controller:
Separate interrupt handling for each module.

VMEbus connection:
A24/D16 Slave interface
D08(O) Interrupter

Power supply:
+5VDC (+-5%), typical 300mA (without modules)
+12VDC, 0mA (without modules)
-12VDC, 0mA (without modules)

Temperature range:
Operating: 0..+60 degr. Celsius
Storage: -20..+70 degr. Celsius

Humidity:
Class F, non-condensing.